

ONS00149
09/817,330

Amendments to the Claims

Claims 1-18 (canceled).

19. (currently amended): A method of making an integrated circuit, comprising the step of plating a conductive material to project outwardly from a second surface of a substrate to form a lead-free first lead of the integrated circuit, wherein the lead-free first lead projects outwardly a distance from the second surface between about 50 microns to about 125 microns.

20. (previously presented): The method of claim 19, further comprising the step of mounting a semiconductor die to a first surface of the substrate.

21. (previously presented): The method of claim 20, further comprising the step of forming a signal path on the first surface with the conductive material.

22. (previously presented): The method of claim 21, further comprising the step of disposing the conductive material in a via defined by the substrate to extend the signal path from the first surface to the second surface of the substrate.

23. (previously presented): The method of claim 22, further comprising the step of disposing the conductive material on the second surface to extend the signal path from the via to the lead-free first lead.

ONS00149
09/817,330

24. (previously presented): The method of claim 19, further comprising the step of forming an access pad on the second surface, wherein the access pad comprises the conductive material, and wherein the step of plating the conductive material includes plating the conductive material onto the access pad.

25. (previously presented): The method of claim 24 further comprising the steps of:
disposing a photoresist layer on the second surface;
patterning the photoresist layer to expose the access pad; and
plating the conductive material on the access pad.

26. (previously presented): The method of claim 25, wherein the step of disposing the photoresist layer includes disposing a photoresist layer having a thickness determined by a desired height of the lead-free first lead.

27. (previously presented): The method of claim 19, wherein the step of plating includes the step of plating copper.

28. (previously presented): The method of claim 21, further comprising the step of wire bonding the signal path to a node of the semiconductor die to couple a signal between the node and the lead-free first lead.

29. (previously presented): The method of claim 19, further comprising the step of forming a solder mask on the second surface between the lead-free first lead and a lead-free second lead of the integrated circuit.

ONS00149
09/817,330

30. (previously presented): The method of claim 29, wherein the step of forming includes the step of forming the solder mask after the step of plating.

31. (previously presented): The method of claim 19, wherein the step of plating includes the step of plating the conductive material in an outward direction for routing a current (I_{SIGNAL}) through the lead-free first lead that flows parallel to the outward direction.

32. (previously presented): A method of forming an integrated circuit, comprising the steps of:

providing a substrate having a first surface for mounting a semiconductor die; and

plating a conductive material to extend outwardly from a second surface of the substrate to form a lead-free lead of the integrated circuit.

33. (previously presented): The method of claim 32, wherein the step of plating includes plating copper to form the lead-free lead.

Claim 34 (canceled).

35. (original): The method of claim 33, wherein the step of disposing includes the step of forming the lead to a height that maintains a spacing between the substrate and the motherboard.

ONS00149
09/817,330

36. (currently amended): A method of making an integrated circuit, comprising the steps of:

mounting a semiconductor die to a first surface of a substrate;

disposing a conductive material along the first surface and through a via of the substrate to form a signal path of the integrated circuit between the first and a second surface of the substrate; and

plating the conductive material on the second surface to form a lead-free lead of the integrated circuit that is electrically coupled to the signal path, and that projects outwardly from the second surface a distance between about 50 microns and about 125 microns.

Claims 37-38 (canceled).